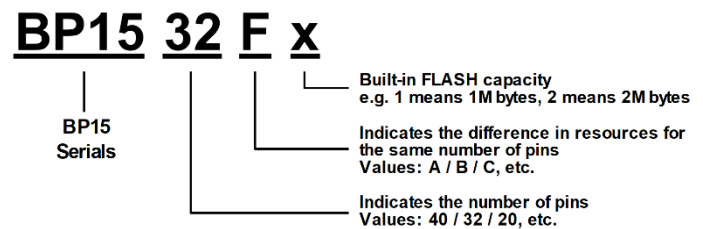


BP1532Fx Datasheet

High Performance 32-bit Bluetooth and 2.4GHz Wireless Audio Processor

Model Naming Analysis



Versions:

Date	Version	Description
2023 / 10	V0.1	Preliminary English version
2024 / 5	V0.2	Revision of overview, pin description and chip usage conditions
2024 / 10	V0.3	Add model naming analysis

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1. Overview

Core and Memory

- High performance 32-bit RISC core, supports DSP instruction, with floating-point unit(FPU) integrated
- FFT/IFFT accelerator supports operations of up to 1024 complex numbers or 2048 real numbers
- 256KB on-chip SRAM, I-Cache and D-Cache support XIP operation
- Internal FLASH for code and data storage
- EFUSE configuration register
- 2-wire SDP(Serial Debug Port), break-point and code tracking debug
- 41 interrupt vectors and 4-level interrupt priority

Audio

- Three 24bit audio ADC, $SNR \geq 102dB$, 9 sampling rate: 8KHz / 11.025KHz / 12KHz / 16KHz / 22.05KHz / 24KHz / 32KHz / 44.1KHz / 48KHz
- Support 1 analog microphone, single-ended input with AGC
- Support 1 analog LINE-IN input
- Two 24bit audio DAC, $SNR \geq 105dB$, 13 sampling rate: 8KHz / 11.025KHz / 12KHz / 16KHz / 22.05KHz / 24KHz / 32KHz / 44.1KHz / 48KHz / 88.2KHz / 96KHz / 176.4KHz / 192KHz
- Directly drive earphone of 16 Ω or 32 Ω with power of 40mW
- One duplex I2S (or IIS), sampling rate 8K~192KHz, max. 32bits, and support 4-channel TDM input
- One S/PDIF with receive or transmit, supporting HDMI ARC

Bluetooth

- Dual mode Bluetooth V5.3, supporting BR, EDR and BLE
- Support BLE Audio, including CIS and BIS
- Support Piconet and Scatternet networking protocols
- Maximum transmit power is 8dBm, support class1, class2 and class3
- Receiving sensitivity (typical)
DH1: -92dBm
2DH5: -92dBm
BLE 1M: -95dBm
BLE 2M: -92dBm
- Support
A2DP/AVRCP/HFP/HSP/OPP/HID/SPP/PBAP/GATT/SM profiles
- Support PLC (Package Loss Concealment)

2.4GHz Wireless Audio

- Use GFSK bi-directional link communication
- Support 1 / 2M rate
- Support high quality and low latency wireless audio bi-directional transmission with latency as low as 10ms or less

Power, Clock and Reset

- DC 3.0~5.5V power supply @ LDOIN
- Support single power supply with built-in DCDC and multiple LDOs
- RC 12MHz and two PLL clocks
- Support 24MHz crystal
- Internal POR(Power on Reset), LVD(Low-Voltage-Detection) and Watchdog
- Multiple low-power options: CPU clock frequency reduction, system clock frequency reduction, sleep, deep sleep

Timer, PWM and PWC

- 4 basic timers (TIM1, TIM2, TIM3, TIM4)
- 4 general timers (TIM5, TIM6, TIM7, TIM8), with PWM and PWC function

Peripherals

- Max. 12 GPIOs
- All GPIOs support external interrupt and wakeup
- GPIOs configurable: pull-up, pull-down, Hi-impedance, pull-down current source, etc
- USB 2.0 Full-speed OTG controller and PHY, 6 endpoints
- One CAN bus supporting CAN 2.0A / B
- One SDIO @ max.30M
- One duplex UART1 @ max.3Mbps
- 12-bit SAR-ADC @ max. 450K sampling rate, sampling from 9 external IOs or 5 internal voltages
- One IR interface, supports NEC or SONY mode

DMA

- 6-channel DMA, all memory direct addressing, addresses can be assigned to any peripherals except OTG, CAN, IR and I2C
- Unique automatic transmit-and-capture mechanism for memory and IO matching, or DMA-GPIO, can simulate various communication and controlling timing

SDK Firmware Stack and IDE

- Audio algorithm list:
Decode: MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV(IMA-ADPCM & PCM), AIF, AIFC
Encode: MP2, MP3, IMA-ADPCM
- Sound effects:
Echo, Reverb, 3D, Virtual bass, Auto-tune/pitch shifter/Voice changer, EQ, DRC, AEC, Noise

suppression, Frequency-shifting, Screaming detection and suppression

- Support 24-bit high-precision DSP sound processing
- SDK includes abundance of examples and middleware
- Free Eclipse-based IDE and GCC compiler
- Support FreeRTOS
- All C programming, easy for porting
- Graphical real-time tuning tool

Firmware Programming and Protection

- Multiple flash programming supported: debugger, specific burner/programmer, or Flash Burner Lite
- Firmware upgradable with Dual-bank
- 32-bit customized key for firmware encryption
- On-chip 64-bit unique ID

ESD

- HBM 2KV ESD capability

Package and Operational Temperature

- QFN32 (4mm x 4mm)
- Working temperature: -40°C ~ 85°C

Application Fields

- Bluetooth audio speaker, Party Boxes and Soundbar Products, etc.
- Bluetooth sports headset, gaming headset, etc.
- 2.4G wireless audio transmission applications
- All kinds of Bluetooth audio and voice application products

2. Functional Block Diagram

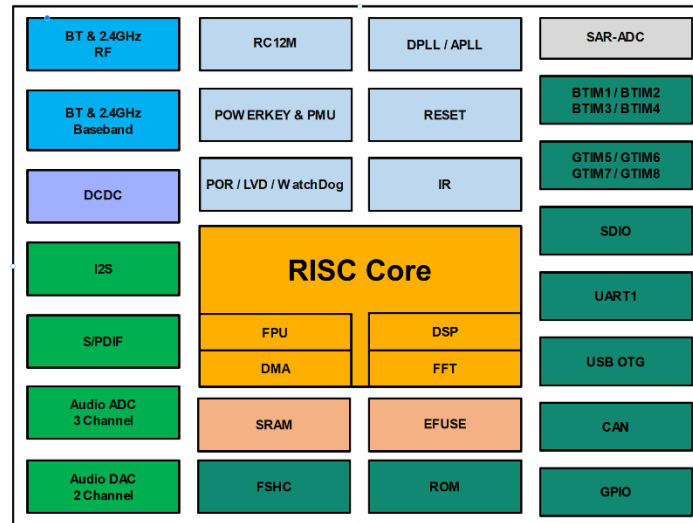


Figure 1. Functional Block Diagram

3. Pin Definition

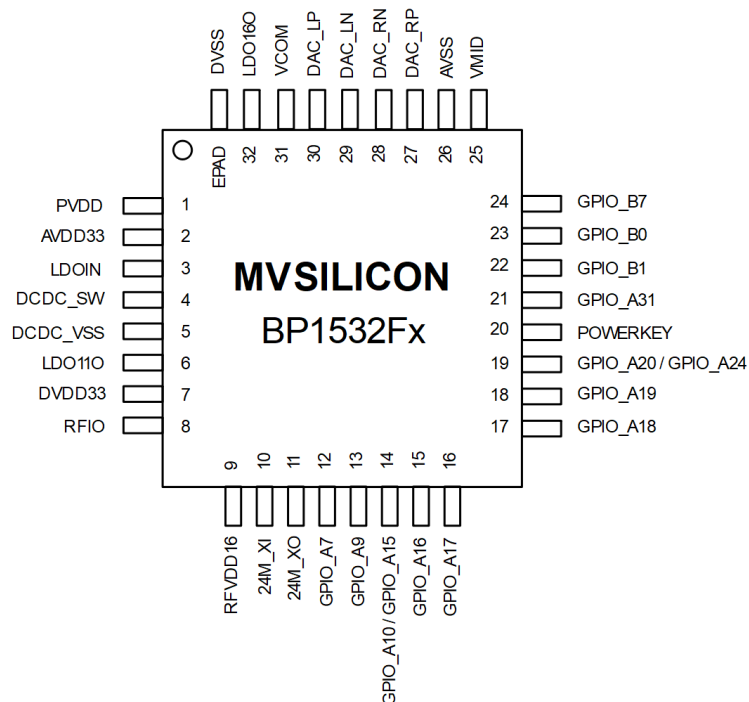


Figure 2. Pin Definition

4. GPIO Pin Description

Table 1. Pin definition

Pin#	Pin Name	Type	Other multiplexing function(s)
1	PVDD	PWR	DAC's internal power driver section, connected to DVDD33 or LDO16O depending on the application, external filtering capacitor is required
2	AVDD33	PWR	Analog power output, external filter capacitor is required
3	LDOIN	PWR	Power input for whole chip
4	DCDC_SW	PWR	Built-in DCDC SW pin, connected to external power inductor
5	DCDC_VSS	GND	Built-in DCDC ground pin, connected to digital ground
6	LDO11O	PWR	1.1V core power, external filter capacitor is required
7	DVDD33	PWR	Digital power output, external filter capacitor is required
8	RFIO	AIO	RF antenna port
9	RFVDD16	PWR	RF power 1.6V output, external filter capacitor is required
10	24M_XI	I	24M crystal XI
11	24M_XO	O	24M crystal XO
12	GPIO_A7	I/O	AD0 / SPIM_MISO / UART0_CTS / UART0_RTS / I2S1_LRCK / MCLK1_OUT / MCLK1_IN / TIM5_PWM
13	GPIO_A9	I/O	AD0 / SPIM_CS / CAN_TXD / UART1_RXD / I2S1_BCLK / TIM6_PWM
14	GPIO_A10 / GPIO_A15	I/O	AD0 / CAN_RXD / UART1_TXD / I2S1_DO / I2S1_DI / TIM5_PWM / TIM6_PWM / LEDC6 / AD0 / SD_DAT / LEDC7
15	GPIO_A16	I/O	AD0 / SD_CLK
16	GPIO_A17	I/O	AD0 / SD_CMD
17	GPIO_A18	I/O	OTG_DM / UART1_RXD / UART1_TXD
18	GPIO_A19	I/O	OTG_DP / UART1_TXD / UART1_RXD
19	GPIO_A20 / GPIO_A24	I/O	AD0 / SD_DAT / UART1_TXD / I2S1_LRCK / TIM7_PWM / AD2 / UART1_TXD / MCLK0_OUT / MCLK0_IN / TIM5_PWM / TIM6_PWM / LEDC_CLK
20	POWERKEY	I	Configurable power control pin with ADC function
21	GPIO_A31	I/O	AD6 / SPDIF_AI / FUSE_VDD25 / UART1_TXD / I2C_SCL / I2S1_DI / I2S1_DO / SPDIF0_DI / SPDIF0_DO / DMIC_CLK / SPDIF1_DI / SPDIF1_DO / IR_IN
22	GPIO_B1	I/O	ADC7 / LINEIN2_L / TIM5_PWM / TIM6_PWM / SW_DATA
23	GPIO_B0	I/O	ADC7 / LINEIN2_R / TIM5_PWM / TIM6_PWM / SW_CLK
24	GPIO_B7	I/O	MICIN_P
25	VMID	AO	Bias voltage for audio module internal use
26	AVSS	GND	Analog ground
27	DAC_RP	AO	Audio R-channel differential P-side output
28	DAC_RN	AO	Audio R-channel differential N-side output
29	DAC_LN	AO	Audio L-channel differential N-side output
30	DAC_LP	AO	Audio L-channel differential P-side output
31	VCOM	AO	DAC output common-mode level
32	LDO16O	PWR	Digital 1.6V power output, external filter capacitor is required
33	DVSS	EPAD	Digital and RF ground

Note:

- 1) Pad types:
I: digital input; O: digital output; AI: analog input; AO: analog output; I/O: bi-directional input/output;
PWR: Power; GND: Ground
- 2) All GPIOs are grouped into A, B. Group A has 10 signals and Group B has 3.
- 3) BP1532Fx is a CMOS device and all unconnected GPIO pins are supposed to be set to pull-up or pull-down in order to avoid the unnecessary power consumption cause by the electric charge accumulation.
- 4) GPIOs response differently with the different type of resets:
 - a) If Power-on-Reset (POR) is active, GPIOs will be reset as input and be set to high-impedance as indicated in table 2.
 - b) If Watchdog reset or software SYSTEM RESET is active, GPIOs, based on the register configuration, can either keep the previous status(multiplexing, input/output or pull-up/down setting) before the reset or be set as the same as described in a) or table 2.

Table 2. GPIO State and Electric level (POR)

Pin(s)	Type	Electric level
All GPIOs	Floating	High Impedance

- 5) MCLK1 is used for connected to other audio peripherals as audio clock, which can be configured as input (IN) or output (OUT).
- 6) If the POWERKEY is not used, please keep the pin floating, and NOT to short the POWERKEY to GND or LDOIN.
- 7) The GPIO_B7 and GPIO_B[1:0] are always have pull-down resistors of about 41 K Ω . When these IOs are set to the SAR-ADC function, consider their effect on the ADC sampling results. When set to other digital interfaces, please consider the corresponding impedance matching requirements.

5. Electrical Characteristics

5.1. Working condition

Table 3. Working Condition

Parameter	Pin	Min	Typ	Max	Unit
Ambient temperature		-40		85	°C
Power supply for chip	LDOIN	3.0		5.5	V
Power supply for analog modules	AVDD33		3.3		V
Power supply for digital 3.3V modules	DVDD33		3.3		V
Power supply for digital 1.6V modules	LDO16O		1.6		V
Core working voltage	LDO11O		1.1		V
Audio bias voltage	VMID		1.65		V

5.2. Digital IO Electrical Characteristics

Table 4. Digital IO DC Characteristics

Symbol	Meaning	Min.	Typ.	Max.	Unit	Testing Condition
VIH	Input High	2.2		3.6	V	DVDD33=3.3V
VIL	Input Low	-0.3		1.0	V	DVDD33=3.3V
IL	Input leakage current	-10		10	μA	
VOH	Output High	3.0			V	@IOH=8mA
VOL	Output Low			0.3	V	@IOL=8mA

Table 5. Digital IO Driving and Pull-Up/Down Capability

Name	IOs	Option	Unit	Testing Condition
Driving Capability	All GPIOs	4 / 8 / 12 / 24	mA	DVDD33=3.3V, typical
Pull-up	All GPIOs	10 / 100	KΩ	DVDD33=3.3V, typical
Pull-down	GPIO_B7 / GPIO_B[1:0]	41	KΩ	DVDD33=3.3V, typical
	Other GPIOs	20	μA	
Pull-down current source	All GPIOs	1.6 / 3.2 / 4.8	mA	DVDD33=3.3V, typical

Note: The GPIO_B7 and GPIO_B[1:0] are always have pull-down resistors.

5.3. Audio Performance

Table 6. Audio DAC single-ended output performance @ 48KHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		16	24	24	bits
Sampling frequency		8	48	192	KHz
Dynamic Range	@Fin=1KHz, -60dBFS, A-Weighted		105		dB

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	@Fin=1KHz, 0dBFS, A-Weighted		105		dB
THD+N	@Fin=1KHz, A-Weighted		-87		dB
Full Scale Output Signal Level	@Fin=1KHz, 0dBFS		1.07		Vrms
Group Delay			2.17		ms
Phase deviation			0.105		degree
Channel Separation	@Fin=1KHz, 0dBFS		-109.3		dB

Table 7. Audio DAC differential output performance @ 48KHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		16	24	24	bits
Sampling frequency		8	48	192	KHz
Dynamic Range	@Fin=1KHz, -60dBFS, A-Weighted		106		dB
SNR	@Fin=1KHz, 0dBFS, A-Weighted		106		dB
THD+N	@Fin=1KHz, A-Weighted		-87		dB
Full Scale Output Signal Level	@Fin=1KHz, 0dBFS		1.07		Vrms
Group Delay			2.12		ms
Phase deviation			0.101		degree
Channel Separation	@Fin=1KHz, 0dBFS		-120		dB

Table 8. Audio ADC performance @LINEIN channel, 48KHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		16	24	24	bits
Full Scale input Signal Level	AVDD=3.3V		1.0		Vrms
Sampling frequency		8	48	48	KHz
PGA Gain Range		-17.9		18.3	dB
Input Resistance		3		30	KΩ
Dynamic Range	@Fin=1KHz, 1Vrms, A-Weighted		100		dB
SNR	@Fin=1KHz, 1Vrms, A-Weighted		100		dB
THD+N	@Fin=1KHz, A-Weighted		-88		dB
Group Delay			570		us
Channel Separation	@Fin=1KHz, 0dBFS		-98		dB

Table 9. Audio ADC (MIC single-ended input) performance @ 48KHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		16	24	24	bits
Full Scale input Signal Level	AVDD=3.3V		1.0		Vrms
Sampling frequency		8	48	48	KHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PGA Gain Range		-11.3		26.5	dB
Input Resistance		3		30	K Ω
Dynamic Range	@Fin=1KHz, 1Vrms, A-Weighted		102.5		dB
SNR	@Fin=1KHz, 1Vrms, A-Weighted		102.5		dB
THD+N	@Fin=1KHz, A-Weighted		-88		dB
Group Delay			584		us

Note:

- 1) Audio parameters are based on samples only and were measured at room temperature and pressure, with the development board powered at 5V.

6. Operational Frequency and Power Consumption

6.1. Power Consumption under Typical Mode

Table 10. Power consumption

Typical Mode	Typical Current	Condition
Bluetooth A2DP	14mA	Without load (e.g. headset or speaker), disable all audio effect
Bluetooth HFP	14mA	Without load (e.g. headset or speaker), disable all audio effect
Bluetooth sniff	670uA	Bluetooth sniff interval is 500ms
Deepsleep	300uA	USB Wake-Up ready

Note:

1. Power consumption parameters are only based on samples and measured at normal temperature and atmospheric pressure.
2. Test results depend on the specified hardware environment and software.

7. Package

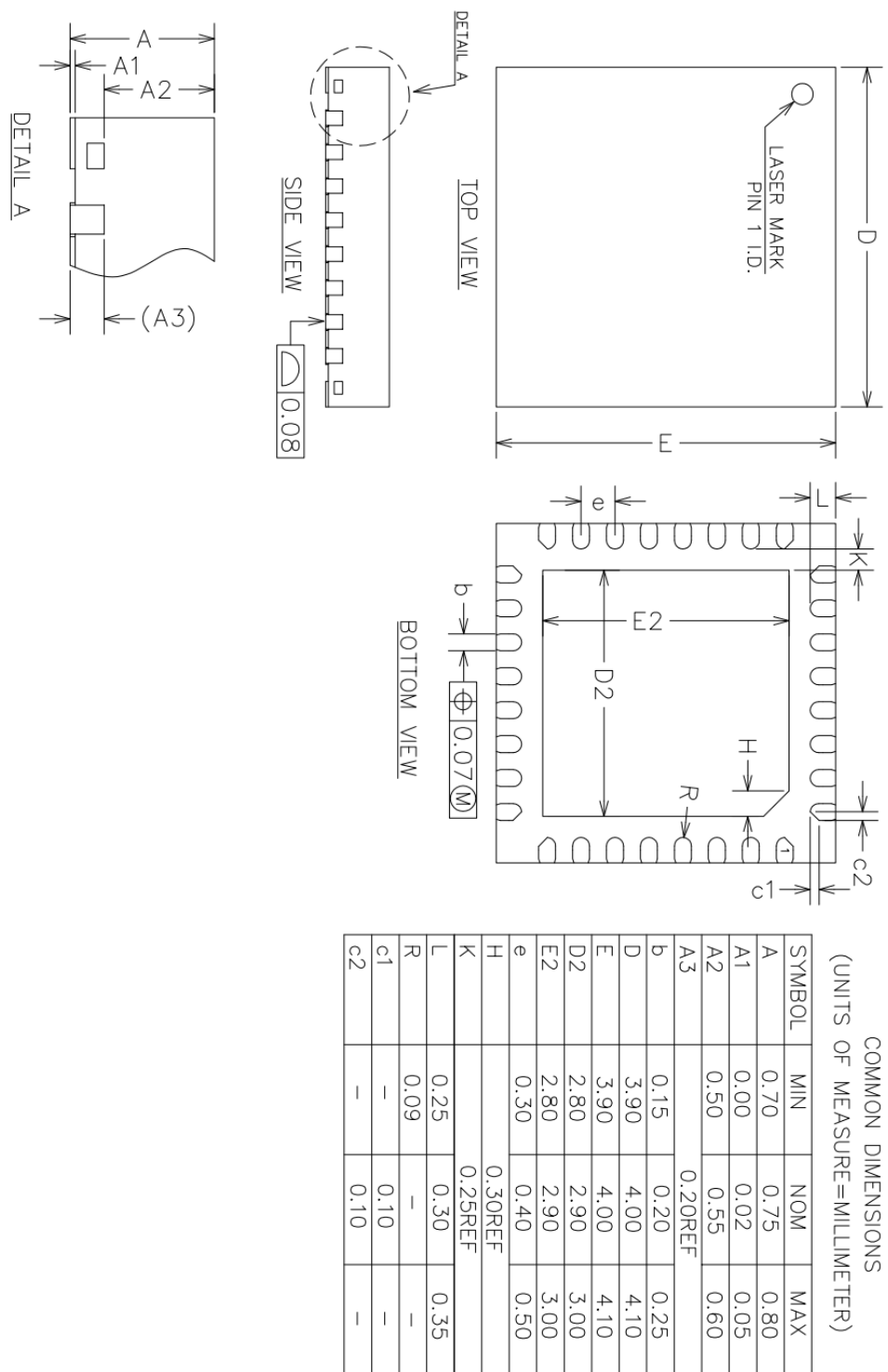


Figure 3. Package and Size

8. Storage and Soldering

Storage temperature: -65°C ~ 150°C.

BP1532Fx is a moisture sensitive component. The moisture sensitivity classification is **Class 3**.

It's important that the parts are handled under precaution and a proper manner.

The handling, baking and out-of-pack storage conditions of the moisture sensitive components are described in IPC/JEDC S-STD-033A.

The Technologies recommends utilizing the standard precautions listed below.

1. Calculated shelf life in Sealed Bag: 12 months at <40°C and <90% relative humidity(RH)
2. Peak Package Body Temperature: 250°C
3. After bag is opened, devices that will be subjected to reflow solder of other high temperature process must be:
 - a. Mounted within 168 hours of factory condition $\leq 30^{\circ}\text{C}$ / 60% RH
 - b. Stored at <10% RH if not used
4. Devices require baking, before mounting if:
 - a. Humidity indicator card is >10% when read at $23\pm 5^{\circ}\text{C}$ immediately after moisture barrier bag is opened
 - b. Items 3a or 3b is not met
5. If baking is required, please refer to J-STD-033 standard for low temperature (40°C) baking requirement in Tape/Reel form.

9. Declaration

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10. Technical Support

Shanghai Mountain View Silicon Co., Ltd. (上海山景集成电路股份有限公司)

Website: <http://www.mvsilicon.com>

Email: support@mvsilicon.com

Shanghai Headquarter:

Suite 4C, Building 3, 1238 Zhangjiang Road, Pudong New District, Shanghai, China

ZIP: 201203

Tel: 86-21-68549851/68549853/68549857

Fax: 86-21-58992765

Shenzhen Sales and FAE Branch:

Suite 6A, Olympic Tower, 2 Shangbao Road, Futian District, Shenzhen, Guangdong, China

ZIP: 518034

Tel: 86-755-83522952

Fax: 86-755-83522957